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METHOD OF ACHIEVING IMPROVED STI GAP FILL WITH REDUCED STRESS

FIELD OF THE INVENTION

001 This invention generally relates to integrated circuit manufacturing processes and more particularly to an improved shallow trench isolation (STI) formation process and structure to form a STI feature with improved gap filling with reduced stress thereby improving charge carrier mobility.

BACKGROUND OF THE INVENTION

002 As devices become smaller and integration density increases, high density plasma chemical vapor deposition (HDP-CVD) has become a key process due in back filling high aspect ratio features such as shallow trench isolation (STI) features due to its superior gap-filling capability. In particular, high density plasma (HDP) processes, such as electron cyclotron resonance (ECR) processes and inductively coupled plasma (ICP) processes have been found to produce high-quality field oxides. Generally, HDP-CVD provides a high density of low energy ions resulting in higher quality films at lower deposition temperatures, compared to other plasma enhanced CVD deposition processes such as PECVD.

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003 In a HDP-CVD deposition process, for example, a bias power is coupled to the semiconductor wafer to attract ions which sputter (etch) the wafer during deposition (re-sputtering effect), thereby preventing a phenomenon known as crowning where the deposition material converges over the trench before an etched feature opening is completely filled with the deposition material. The deposition rate may therefore be more finely tuned to improved CVD deposition properties to, for example, avoid crowning.

004 As device sizes decrease below 0.13 micron critical dimension, however, the gap fill of openings, for example STI openings, becomes problematical and the process window for successful gap filling is narrowed. Generally, as device sizes decrease and aspect ratios increase to greater than about 4 to 1, relatively high plasma RF powers, for example, greater than about 6 Watts/cm² are delivered to a process wafer surface creating relatively large thermal stresses during the gap filling deposition. To maintain lower deposition temperatures the backside of the wafer is frequently cooled, leading to increased thermal gradients and consequently stresses across the wafer surface and through the wafer thickness. Consequently, compressive stresses, relatively larger parallel to wafer process

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surface, are generated following the HDP-CVD process leading to subsequent problems in device quality and reliability. For example, charge carrier mobilities are strongly influenced, e.g., decreased due to stress fields present in semiconductor materials.

005 There is therefore a need in the integrated circuit manufacturing art to develop an improved method for filling gaps including shallow trench isolation (STI) structures as well as a STI structure having reduced stresses to achieve improved semiconductor device quality and reliability.

006 It is therefore among the objects of the present invention to an improved method for filling gaps including shallow trench isolation (STI) structures as well as a STI structure having reduced stresses to achieve improved semiconductor device quality and reliability, in addition to overcoming other shortcomings and deficiencies of the prior art.

SUMMARY OF THE INVENTION

007 To achieve the foregoing and other objects, and in accordance with the purposes of the present invention, as embodied and broadly described herein, the present invention provides a shallow trench isolation (STI) structure and method of forming the same with reduced stress to improve CMOS device charge mobility.

008 In a first embodiment, the method includes providing a semiconductor substrate comprising at least one patterned hardmask layer overlying the semiconductor substrate; dry etching a trench in the semiconductor substrate according to the at least one patterned hardmask layer; forming one or more liner layers to line the trench selected from the group consisting of silicon dioxide, silicon nitride, and silicon oxynitride; forming one or more layers of trench filling material comprising silicon dioxide to backfill the trench; carrying out at least one thermal annealing step to relax accumulated stress in the trench filling material; carrying out at least one of a CMP and dry etch process to remove excess trench filling material above the trench level; and, removing the at least one patterned hardmask layer.

009 These and other embodiments, aspects and features of the invention will be better understood from a detailed description of the preferred embodiments of the invention which are further described below in conjunction with the accompanying Figures.

BRIEF DESCRIPTION OF THE DRAWINGS

0010 Figures 1A-1F are representational cross sectional side views of a portion of a semiconductor device including a STI feature at stages in manufacturing according to an embodiment of the present invention.

0011 Figures 2A-2C are representational cross sectional side views of a portion of a semiconductor device including a STI structure formed according to exemplary embodiments of the present invention.

0012 Figure 2D is a completed CMOS device including STI structures formed according to embodiments of the present invention.

0013 Figure 3 is an exemplary process flow diagram including several embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

0014 According to the present invention a method for improved gap fill is explained with reference to the formation of an exemplary shallow trench isolation (STI) feature and exemplary CMOS device. While the method of the present invention is particularly advantageously applied to the formation of STI features, it will be appreciated that the method of the present invention may be applied to the filling of other types of gaps or openings in an integrated circuit manufacturing process where reduced stresses may advantageously improve charge mobility.

0015 In one exemplary implementation of the present invention, referring to Figure 1A is shown a semiconductor substrate 12, for example single crystalline or polycrystalline silicon. It will be appreciated that the substrate may include epi silicon layer, buried layers, silicon on insulator (SOI), SiGe, and GaAs. A pad oxide layer 12A of SiO_2 about 50 Angstroms to about 150 Angstroms is first thermally grown by conventional processes or formed by LPCVD TEOS over the silicon substrate 12 to aid in reducing surface stresses induced in subsequent processing steps. A silicon nitride (e.g., Si_3N_4) layer 14 is then deposited by a CVD method, for example, LPCVD, to a thickness of about 500 Angstroms to about 2000 Angstroms.

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0016 A second hardmask layer 14B may optionally be added as a hardmask for a subsequent dry etch process, for example formed of PECVD SiON, PECVD SiO₂, or LPCVD TEOS. The second hardmask layer 14B may be formed over the SiN layer 14 to a thickness of about 150 Angstroms to about 500 Angstroms. In addition, an organic or inorganic anti-reflective coating (ARC) is preferably formed over the SiN hardmask or second hardmask, if present, to a thickness of about 200 Angstroms to about 1000 Angstroms, depending on the wavelength of light to be used in the photolithographic process. For example, a second hardmask formed of SiON may be deposited to a thickness between about 500 Angstroms and about 1000 Angstroms to function as both an etching hardmask and as an ARC layer.

0017 Still referring to Figure 1A, a photoresist layer 16A, e.g., 1000 to 6000 Angstroms thick is then deposited over the second hardmask/ARC layer 14B and photolithographically patterned to form an opening e.g., 16B exposing a portion of the second hardmask/ARC layer 14B for dry etching through a thickness portion of the second and SiN hardmask layers, e.g., 14B and 14 respectively, to form a dry etching hardmask.

0018 Referring to Figure 1B, the hardmask/ARC layer 14B and SiN hardmask layer 14 are then etched according to the patterned

photoresist layer opening 16B by conventional process to expose a portion of the substrate 12 to form hardmask opening 16C according to a conventional reactive ion etch (RIE) process, for example including a fluorocarbon etching chemistry, for example, CF₄. For example, the silicon nitride hardmask layer 14 is anisotropically dry etched through a thickness to include the pad oxide layer 12A to expose a surface portion of the substrate 12 according to endpoint detection.

0019 Referring to Figure 1C, in one aspect of the method of the present invention, following removal of the photoresist layer 16A, for example, by a wet stripping or dry ashing process, a STI trench feature 18 is then dry etched into the silicon substrate to a depth between about 60 Angstroms and about 5000 Angstroms, preferably forming sloped sidewall portions, e.g., 18A having an angle, theta, with respect to the plane of the major surface (process surface) of the substrate preferably between about 80 and 89 degrees, the upper portion of the trench being wider than the bottom portion. A conventional etching chemistry, including for example, Cl₂, HBR, and O₂ is used to dry etch the trench 18 unto the substrate 12 to from a shallow trench isolation (STI) opening (trench opening) 18. Preferably, during the trench etching process, trench top portion corners at e.g., 18B and

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trench bottom portion corners e.g., 18C are formed such that that the trench opening corners at the top and/or bottom corner portions of the trench are rounded e.g., having a radius of curvature. Such STI trench corner rounding is advantageous for preventing undesirable electrical behavior such as high electrical fields affecting voltage threshold (V_T) in a completed CMOS device.

0020 For example, several STI trenches are etched simultaneously in a semiconductor substrate, being spaced between about 0.06 microns and about 0.30 microns, each STI trench and having an upper portion wider than a lower portion, the upper portion width between about 0.03 microns and about 0.20 microns.

0021 Referring to Figure 1D following etching of the trench 18, a conventional cleaning process using SC-1 and SC-2 cleaning solutions is carried out to clean the substrate surface including exposed portions in the STI trench. In another aspect of the invention, one or more layers e.g., 20 are deposited to line the trench opening. For example in one embodiment, the one or more liner layers including at least one of thermal oxide (SiO_2), silicon nitride (e.g., SiN , Si_3N_4), and silicon oxynitride (e.g., $SiON$), including for example, one of an SiO_2/SiN , $SiO_2/SiON$,

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$\text{SiO}_2/\text{SiN}/\text{SiON}$, and $\text{SiO}_2/\text{SiON}/\text{SiN}$ stack having a total thickness of about 30 to about 200 Angstroms. For example, in the case of a silicon substrate, a single layer of thermal oxide may be grown by conventional thermal processes over silicon exposed portions of the trench 18 to form a substantially conformal layer of about 30 Angstroms to about 200 Angstroms in thickness. For example, the thermal oxide is grown at a temperature of about 900 °C to about 1150 °C in a conventional furnace or RTP apparatus. In one embodiment, the thermal oxide layer is treated with N_2 to form an uppermost layer of SiN , for example by treating the thermal oxide in ambient N_2 at a temperature of from about 800 °C to about 1000 °C, or carrying out a nitrogen atom implant process, e.g., plasma immersion or ion implantation, followed by annealing at greater than about 600 °C.

0022 In another embodiment, an LPCVD, PECVD, or ALCVD process is carried to blanket deposit a silicon nitride or silicon oxynitride layer over a thermal oxide to form the trench liner 20. Alternatively, trench liner 20 may be formed of single or multiple layers of SiN and SiON which are deposited without first forming the thermal oxide. However, forming the thermal oxide is preferred in the case a silicon substrate is used, since it tends to better repair any damage caused by etching and to relax

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thermally induced stresses at the trench surface. In the case, the substrate is not silicon, for example GaAs, the oxide layer may be formed by LPCVD or ALCVD over the exposed substrate portions within the STI trench, prior to forming SiN and/or SiON overayers. For example, SiN is preferably formed by a LPCVD, PECVD, or ALCVD process by reacting silane (SiH₄) and NH₃ at about 400 °C to about 800 °C. Silicon oxynitride (e.g., SiON) is preferably formed by reacting silane (SiH₄), NH₃, oxygen (O₂) and/or N₂O at deposition temperatures of about 350 °C to about 800 °C.

0023 In one embodiment the trench liner is formed of a triple layer of SiO₂/SiN/SiON or SiO₂/SiON/SiN, for example by a first oxide formation process, e.g., thermal growth, ALCVD, ALCVD, followed by an LPCVD, PECVD, or ALCVD, preferably an LPCVD or ALCVD process to deposit SiN and/or SiON. It will be appreciated that the term SiN is intended to include the various stoichiometries of silicon nitride, e.g., Si_xN_y, including Si₃N₄. In addition, the term SiON is intended to include the various stoichiometries of silicon oxynitride e.g., Si_xO_yN_z. Following the formation of the trench liner 20, preferably a thermal annealing process is carried out to relax thermally induced stresses formed by previous trench liner 20 formation processes,

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for example using a furnace or RTP process at 500 °C to 1100 °C in either ambient O₂ or N₂.

0024 According to another aspect of the invention, one or more layers of SiO₂ are blanket deposited to backfill the trench to produce a reduced stress trench filling material compared to conventional HDP-CVD methods. Preferably the trench filling material layers are formed of undoped silicate glass (USG) and/or SOG. Preferably the USG is formed by reacting tetraethylorthosilicate (TEOS) and ozone (O₃) or silane (SiH₄) and O₂. Preferably, the USG deposition process includes sub-atmospheric pressure CVD (SACVD), atmospheric pressure CVD (APCVD), and/or high density plasma CVD (HDPCVD) at a deposition temperature from about 400 °C to about 800 °C. The SOG may be organic or inorganic spin on glass (SOG) e.g., preferably including siloxane or silicate precursors, respectively. Preferably, the SOG precursor comprises flowable mixtures including cross-linking agents to form cross-linked polymers, followed by a curing process at about 350 °C to about 450 °C to form cross-linked SiO and/or SiO₂ groups. Alternatively, polysesilquioxanes may be used followed by a curing process of about 100 °C to about 175 °C.

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0025 Referring to Figure 2A, in one embodiment of the present invention, the STI trench 18 is backfilled completely with a single layer 22 of one of an organic or inorganic SOG (following curing), or SACVD or APCVD USG. In an important aspect of the invention, an annealing process is then carried out at a temperature of about 500 °C to about 1100 °C to relieve any stresses created by the deposition process. Preferably, the annealing process is carried out in an ambient O₂ and/or N₂ containing atmosphere for 10 seconds to about 3 hours in a furnace for treating multiple wafers or RTP (rapid thermal process) apparatus for treating single wafers as is known in the art. In addition, a low compressive stress HDP-CVD process may be used to deposit USG followed by the stress reducing annealing process according to preferred embodiments to form a stress relaxed STI structure.

0026 Referring to Figure 2B, in another embodiment, multiple layers of SiO₂ are deposited to backfill the STI trench. For example, a first layer 26A of SOG is deposited by a spin on process followed by a curing process to fill the STI trench to less than or equal to half the STI trench depth. A USG layer, e.g., 26B is then deposited using TEOS and O₃ or SiH₄ and O₂ by an SACVD, APCVD, or HDPCVD process at about 400 °C to about 800 °C.

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Advantageously, during the CVD process residual stresses formed by the SOG layer 26A during the curing and shrinking process are released. Preferably, in an important aspect of the invention, following the CVD process, an additional annealing process is carried out at a temperature of about 500 to about 1100 C to further relieve any stresses in the deposited SOG/SiO₂ layers. It will be appreciated that the order of depositing the layers may be reversed, however is less preferred due to the tendency of the SOG to absorb moisture.

0027 Referring to Figure 2C, in another embodiment, a plurality of trench filling layers are formed with one or more CVD USG layers, e.g., SACVD, APCVD, or HDPCVD, together with one or more SOG layers, with an optional annealing process performed between each layer deposition, but at least following deposition of the uppermost trench filling layer. For example, a first layer 28A of CVD USG or SOG (including a curing process) is deposited to about less than about 1/2, e.g., about 1/3 the depth of the trench by a first deposition using a CVD process or SOG process (including a curing process) followed by an annealing process according to preferred embodiments. A second layer 28B of CVD USG or SOG (including a curing process) is then deposited to about the same thickness followed by a second annealing

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process. A third layer e.g., 28C of CVD USG or SOG (including a curing process) is then deposited to a final thickness e.g., the deposited layers having a total thickness of from about 2000 to about 8000 Angstroms, followed by a third annealing process. Preferably, a HDP-CVD process is used for only the second and subsequent deposited layers e.g., 28B, 28C layers following initial depositions e.g., first and second layers of SOG or APCVD or SACVD, to reduce the possibility of void formation. In addition, with multiple layers being formed of SOG oxide, SACVD oxide (USG) and/or APCVD oxide (USG), an annealing process between layer depositions may be optionally foregone, the annealing process be carried out following deposition of the final oxide layer.

0028 Still referring to Figure 2C, in another embodiment, the initial layer e.g., first layer 28A of CVD USG is deposited to fill less than about 1/2 the depth, e.g., about 1/3 of the STI trench using e.g., SACVD, APCVD or HDP-CVD, followed by an optional-annealing process according to preferred embodiments. The second layer, e.g., layer 28B, is formed of SOG formed to about the same or greater thickness following a curing process. The third layer, e.g., 28C of CVD USG is then deposited to form the final thickness by e.g., e.g., SACVD, APCVD or HDP-CVD,

followed by an annealing process according to preferred embodiments.

0029 According to preferred embodiments for forming a reduced (relaxed) stress STI oxide filling, it has been found that MOSFET device performance is improved. For example, by reducing stresses in the length and width directions of the STI oxide, e.g., in the plane of the semiconductor substrate, charge carrier mobility, including electrons and holes in N and PMOS devices, respectively, is improved in adjacent semiconductor material portions. The improvement in charge carrier mobility shows improvement particularly in the case of subsequent formation of self aligned metal silicides (salicides), e.g., CoSi_2 , NiSi , and TiSi_2 , over source/drain regions of the semiconductor substrate, including e.g., silicon epitaxially grown (SEG) raised source/drain regions. For example referring to Figure 2D is shown an exemplary MOSFET device having STI regions 32A and 32B formed according to preferred embodiments in semiconductor substrate 12, followed by conventional processes to form S/D doped regions e.g., 34A, a polysilicon gate structure 36 with gate oxide 37, oxide and/or nitride spacers e.g., 38, SDE doped regions 34B, and salicide regions e.g., 36A, 36B, formed over raised S/D silicon epitaxial growth (SEG) regions e.g., 38A and

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38B, as well as an upper portion of the polysilicon gate structure, e.g. 36C. The improved charge carrier mobility in the S/D regions adjacent the relaxed oxide filled STI structures 32A and 32B, for example, reduces sheet resistance, allowing shallower junction depths (e.g., SDE regions) to be formed, including raised S/D regions, improving device performance and reliability. For example I_{dsat} is improved by improved charge carrier mobility enabled by relaxed oxide filled STI structures. It will be appreciated that the relaxed oxide filled STI structure formation process may be advantageously used with other device technologies including substrates including strained Si, silicon on insulator (SOI), and SiGe as well as the formation of advanced MOSFET structures such as finFET devices.

0030 Referring back to Figure 1D, following blanket deposition of SiO_2 (STI oxide) e.g., 22 to backfill the STI trench 18 according to the preferred embodiments, a planarization process according to one of a dry etchback and CMP process is carried out where excess oxide above the trench level, including any hardmask layers above the SiN hardmask 14, is removed. For example, a portion of the STI oxide layer may be photolithographically patterned and partially removed by a conventional dry etchback process, followed by a conventional CMP process to remove any

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remaining excess oxide and hardmask layers above the SiN hardmask layer 14. For example, preferably, the CMP process is carried out at a removal rate of about 1000 Angstroms to about 5000 Angstroms/min and the dry etchback process is carried out at an etch rate of about 1000 to about 10000 Angstroms/min.

0031 Referring to Figure 1E, the SiN layer 14 is then removed by a conventional wet e.g., hot H₃PO₄, etching process or a dry SiN etchback process followed by a pad oxide layer 12A wet stripping process, for example using dilute HF, to leave a portion of the STI oxide layer e.g., 32 extending above the substrate 12 and having an inward edge e.g., 32A extending higher than an outward edge e.g., 32B.

0032 Referring to Figure 3 is shown a process flow diagram including several embodiments of the present invention. In process 301 a semiconductor substrate is provided. In process 303, dielectric layers, including one or more hardmask layers is provided on the semiconductor substrate. In process 305, the one or more hardmask layers are patterned for etching STI trenches into the semiconductor substrate. In process 307, an STI trench feature is etched according to preferred embodiments. In process 309, one or more liner layers are formed to line the STI trench

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opening according to preferred embodiments. In process 311 an annealing process to relax stress in the liners is carried out. In process 313, one or more SiO₂ (USG and/or SOG) layers are deposited according to preferred embodiments. In process 315 an annealing process is carried out to relax stress in the STI oxide filling. In process 317, a planarization e.g., one of a CMP process and dry etch back process, is carried out to remove excess STI oxide and dielectric layers above the one or more e.g., SiN hardmask layer. In process 319, one of a wet or dry etchback process is carried out to remove the SiN hardmask layer leaving an upper portion of the STI oxide protruding higher than the semiconductor substrate level.

0033 The preferred embodiments, aspects, and features of the invention having been described, it will be apparent to those skilled in the art that numerous variations, modifications, and substitutions may be made without departing from the spirit of the invention as disclosed and further claimed below.